Applicant claims an improved semiconductor device having a pair of element formation regions separated by an element isolation region. The device employs a pair of gate electrodes containing impurities of different conductivity types. Connected to the gate electrodes are a pair of impurity storage regions arranged in a direction different from the direction of the arrangement of the gate electrodes. The impurity storage regions can be physically connected to each other by a semiconductor layer. The semiconductor layer can be formed of polycrystalline silicon, and the gate electrodes and impurity storage regions can be formed by selectively implanting impurities to the polycrystalline silicon layer. The width of the semiconductor layer can be a value allowing mask misalignment when forming the pair of gate electrodes and impurity storage regions. The element isolation region can be buried in a trench formed of a boundary between the element formation regions. The element isolation region can isolate the element formation regions comprised of semiconductor layers formed on an insulation layer. The element isolation region can be buried in a trench formed in the semiconductor layers. The widths of the impurity storage regions can be equal to the gate length of the gale electrodes and the lengths of the impurity storage regions can be longer than the gate length.

As amended, applicant recites those embodiments that were recited in claim 11 of the application as originally filed. These are the embodiments where the widths of said first and second impurity storage regions (Fig. 3, L_{diff}) are equal to the gate length of said first and second gate electrodes (Fig. 3, L_G) and the lengths of said first and second impurity storage regions (Fig. 3, $L_H + L_G$)(Appl., p. 11, line 21) are longer than said gate length.

The examiner previously rejected claim 11 under 35 U.S.C. § 103 as obvious in light of Jung. Reconsider is respectfully requested. Jung would not have suggested a semiconductor device having first and second impurity storage regions where the widths of said first and second impurity storage regions are equal to the gate length of said first and second gate electrodes. As can be seen in FIG. 1 of Jung, the widths of the "impurity storage regions" (1/2" in the drawing) are considerably wider that the width of the first and second gate electrodes (3/16" and 1/8", respectively). Jung actually teaches away from semiconductors having "impurity storage regions" as narrow as the gate electrodes. Instead, the regions described by Jung must each be sufficiently wide to provide for contact holes. Therefore, Jung would not have made obvious any of the pending claims.

CONCLUSION

In light of the foregoing amendments and remarks, it is believed that the application is in condition for allowance, so that a prompt and favorable response is respectfully solicited.

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May 27, 2003

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Date Kathleen Gaines

Version with Marking Showing Changes Made

Claim 1 has been amended as follows:

1. (amended three times) A semiconductor device comprising:

a first element formation region in which a device of a first conductivity type is formed;

a second element formation region separated from said first element formation region by an element isolation region and in which a device of a second conductivity type different from said first conductivity type is formed;

a first gate electrode provided on said first element formation region and containing an impurity of the first conductivity type;

a second gate electrode provided on said second element formation region facing said first gate electrode and containing an impurity of the second conductivity type;

a first impurity storage region containing said first conductivity type impurity, having one end connected to an end of said first gate electrode, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes; and

a second impurity storage region, physically connected to said first impurity storage region by a semiconductor layer, said second impurity storage region containing said second conductivity type impurity, and having one end connected to an end of said second gate electrode, having the other end electrically connected to the other end of said first impurity storage region, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes,

the widths of said first and second impurity storage regions are equal to the gate length of said first and second gate electrodes and the lengths of said first and second impurity storage regions are longer than said gate length.

9. (amended) A semiconductor device as set forth in claim [2] 1, wherein:

said semiconductor layer is formed by polycrystalline silicon and said first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to said polycrystalline silicon layer.

10. (amended) A semiconductor device as set forth in claim [2] 1, wherein the width of said semiconductor layer physically connecting said first and second impurity storage regions is a value allowing mask misalignment when forming said first and second gate electrodes and first and second impurity storage regions.